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IN THE CLAIMS

(Currently Amended) For use with an integrated circuit (IC) having a testing port, a

system for securing said IC as against subsequent reprogramming, comprising:

port inhibit circuitry located on said IC and modifiable to achieve a configuration that

determines an extent to which said testing port is enabled, said extent selected from the group

consisting of:

fully enabled,

only partially enabled, and

completely disabled; and

port access circuitry, coupled to said testing port, that enables said testing port based on said

configuration.

2. (Original) The system as recited in Claim 1 wherein said testing port is a Joint Test

Action Group (JTAG) port.

3. (Original) The system as recited in Claim 1 wherein said port inhibit circuitry

comprises an inhibit bit in a one-time programmable register.

4. (Original) The system as recited in Claim 1 wherein said port inhibit circuitry is

configured to be permanently modified prior to delivering said IC to a user thereof.

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(Original) The system as recited in Claim 1 wherein said testing port comprises a

direct loopback between input and output pins thereof.

(Original) The system as recited in Claim 1 wherein said IC is a baseband chip of a

mobile communication device.

8. (Currently Amended) For use with an integrated circuit (IC) having a testing port, a

method of securing said IC as against subsequent reprogramming, comprising:

modifying port inhibit circuitry located on said IC to achieve a configuration that determines

an extent to which said testing port is enabled, said extent selected from a group consisting of:

fully enabled,

only partially disabled, and

completely disabled; and

enabling said testing port based on said configuration.

(Original) The method as recited in Claim 8 wherein said testing port is a Joint Test

Action Group (JTAG) port.

10. (Original) The method as recited in Claim 8 wherein said port inhibit circuitry

comprises an inhibit bit in a one-time programmable register.

11. (Original) The method as recited in Claim 8 wherein said modifying comprises

permanently modifying said port inhibit circuitry prior to delivering said IC to a user thereof.

Canceled

13. (Original) The method as recited in Claim 8 wherein said testing port comprises a

direct loopback between input and output pins thereof.

(Original) The method as recited in Claim 8 wherein said IC is a baseband chip of a

mobile communication device.

15. (Currently Amended) An electronic device, comprising:

an integrated circuit (IC), including:

a testing port,

port inhibit circuitry located on said IC and modifiable to achieve a configuration that

determines an extent to which said testing port is enabled, said extent selected from the group

consisting:

fully enabled,

only partially disabled, and

completely disabled, and

port access circuitry, coupled to said testing port, that enables said testing port based on said

configuration.

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16. (Original) The electronic device as recited in Claim 15 wherein said testing port is a

Joint Test Action Group (JTAG) port.

17. (Original) The electronic device as recited in Claim 15 wherein said port inhibit

circuitry comprises an inhibit bit in a one-time programmable register.

(Original) The electronic device as recited in Claim 15 wherein said port inhibit

circuitry is configured to be permanently modified prior to delivering said IC to a user thereof.

Canceled

20. (Original) The electronic device as recited in Claim 15 wherein said electronic device

is selected from the group consisting of:

a mobile telephone,

a PDA,

an MDA,

an MP3 player, and

a set-top box.